A New Full-Chip Verification Methodology to Prevent CDM Oxide Failures

Melanie Etherton (1), Scott Ruth (1), James W. Miller (1), Rishabh Agarwal (2), Rishi Bhooshan (2), Maxim Ershov (3), Meruzhan Cadjan (3), Yuri Feinberg (3), Karthik Srinivasan (4), Norman Chang (4), Youlin Liao (4)

(1) Freescale Semiconductor, Inc., 6501 W William Cannon Dr, Austin, TX 78735 (USA)
tel.: 512-895-2693, email: Melanie.Etherton@freescale.com

(2) Freescale Semiconductor India Pvt. Ltd., Noida Design Center, Plot No 2 & 3, Sector 16A, Noida UP (India)

(3) Silicon Frontline Technology Inc., 595 Millich Drive, Suite 206, Campbell, CA 95008 (USA)

(4) Apache Design, Inc., a subsidiary of ANSYS, Inc., 2645 Zanker Road, San Jose, CA 95134 (USA)

Abstract - This paper describes a new full-chip CDM ESD verification method that enables the evaluation of complete integrated circuits (ICs) for CDM risk. We demonstrate that a robust analysis must comprehend millions of locations of driver-receiver (D/R) pairs on an IC, an accurate model of the grid resistance and an adequate representation of the CDM current distribution.

I. Introduction

Significant progress has been made in recent years with the development of methods and EDA tools for CDM ESD robustness verification of ICs. For example, schematic or netlist based checks are widely used to find supply domain signal crossings and verify that proper ESD protection is present. Previously available tools and methods aimed to verify the CDM robustness of chips either analyze on a full-chip level with significant simplifications (e.g. two-terminal dc current paths) or are focused on the detailed analysis on a small area of the chip [1-4]. When used together, these tools have significantly improved the ability to detect and correct potential CDM issues before product tape-out.

Even though we apply a comprehensive suite of CDM verification tools to ensure ESD robustness of our advanced mixed signal ICs, we have recently seen CDM failures on gate oxides. While such failures are fairly common for unprotected signals crossing supply domains, ours occur on driver-receiver pairs within the same power and ground domain. Since this is not a typical failure location, previous EDA tools for CDM analysis did not detect these issues. The observed failures are associated with large resistances between the D/R local ground which are common and very difficult to avoid in mixed signal ICs, especially when they contain sensitive analog circuits with isolated ground nets. In most cases, however, a large resistance between the local ground of a driver and receiver will not result in CDM damage. Actual failures are caused when a large CDM discharge current moves through the grid in these locations, causing large potential differences between the grounds of the D/R pair. A CDM-focused analysis must therefore take the locations of drivers and receivers, the grid resistance, and a suitable CDM current flow model into account.

In this paper we introduce a new methodology for full-chip CDM simulation that enables the evaluation of millions of D/R pairs on an IC for CDM risk. We demonstrate the viability of this method by applying it to the IC that showed oxide failures, first with a basic implementation in a commercially available IR drop tool and then with two EDA tools developed by established tool vendors.

II. CDM Fails in the Chip Core

CDM ESD damage often occurs at unprotected supply domain signal crossings and for this reason ESD protection is typically added. Recently, we have seen cases where CDM failures occurred at gate oxides connected to signals that were in the same power and ground domain as the drivers. Figure 1 shows the locations of the failing devices on one early product version (top left) and failure analysis (FA) pictures of gate oxide damage (1-4). CDM failures occurred at 500V CDM on IO pins in the NE corner of the chip.

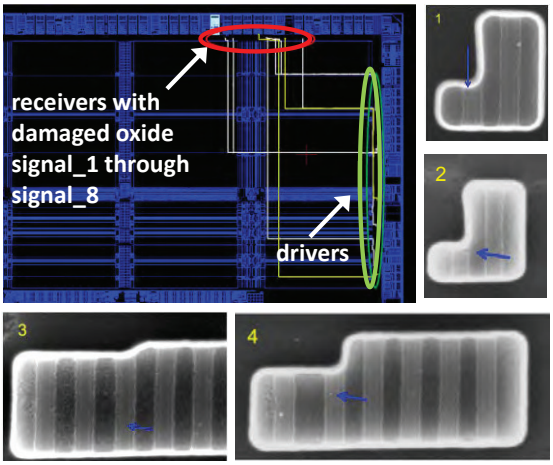

Figure 1: FA results from product showing oxide damage at core devices inside the same power/ground domain after CDM stress.

After detailed analysis, the failure mechanism was determined. The placement and connection of a large IP block in the NE corner of the chip created a high-resistive VSS channel in the area of the damaged buffers (see Figure 2). During a CDM discharge on pins in that corner, the majority of the CDM current flows through that restricted VSS grid, causing a large voltage between the local ground of D/R pairs in that path. The standard IR drop analysis tools did not flag this as a problematic area. The supply voltages during normal operation were within the specified levels.

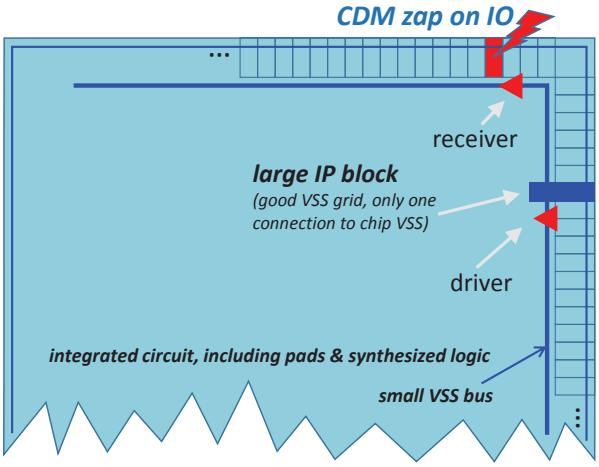

Figure 2: Visualization of the current flow through the die during a CDM discharge that causes damage on the receiver gate.

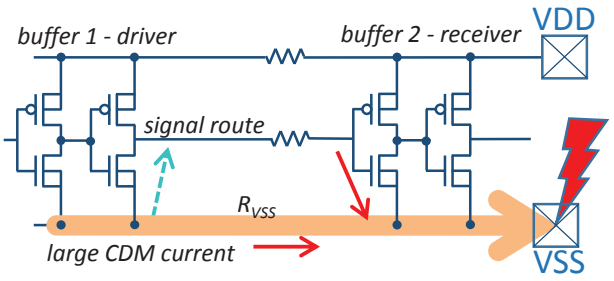

Figure 3: Schematic representation of high resistive ground route.

Figure 3 demonstrates that a combination of large ground resistance and high CDM current can cause an excessive voltage at the gate of a receiving device resulting in oxide damage. The VSS pin is either directly discharged or current is flowing through the VSS net during a CDM discharge on any pin. An 8A current over a 5Ω resistance can result in roughly 40V on the receiver gate. Note that there is no notable CDM current flow in the signal route.

III. CDM Verification Strategy

A. Problem Statement

A large D/R pair ground resistance can be caused by a large distance between them (Figure 4, path B) or by discontinuities in the global ground grid (path A). The latter are common for large mixed-signal chips with sensitive analog IP using several isolated grounds.

The large resistances described are not an ESD issue unless significant CDM discharge currents flow through them. In such case, an excessive voltage drop on any D/R pair ground can result in oxide damage.

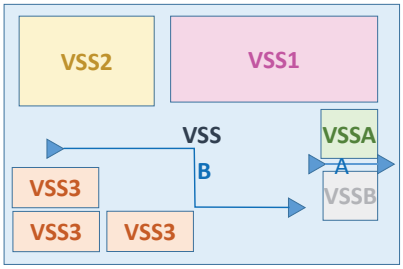

Figure 4: High D/R VSS resistance caused by constriction in the VSS grid (A) or large physical distance between D/R (B).

B. Verification Approaches

Three rule-based automated verification approaches to identify at-risk devices for CDM damage were considered:

D/R route length can be set as constraint or checked with commercially available place and route tools, but they don't correlate with the observed CDM failures.

D/R ground resistance is a good indication for the risk of damage during CDM. A low resistance limit across the complete chip, e.g. 2Ω, results in a low risk for oxide damage. This approach has challenges:

a) Point-to-point ground resistance extractions for all D/R pairs on the IC is not a standard EDA tool feature and computational requirements are high.

b) During a CDM event, the current density varies significantly over the chip. Low resistances are only required in areas with high CDM current densities. Setting low limits for the complete chip may be overkill and can be difficult to implement.

c) Most importantly, the results don't correlate well with the observed CDM failure locations. While it includes information about D/R locations and the grid resistance, it is missing the critical component of the CDM current flow.

D/R ground voltage drop: To accurately identify D/R pairs that are at risk for damage during a CDM event, a realistic representation of the current flow during a CDM discharge must be used. Considering all D/R locations on the chip and simulating a CDM discharge with an accurate representation of the evaluated grid resistance is a complex problem. It requires extensive computational resources (CPU and memory). A simplified approach to solve this problem has to be implemented to enable production use. This approach is discussed in the next section.

IV. CDM Verification Framework

During CDM, every capacitance formed between the package/die and the tester charging plate (Figure 5) is charged/discharged. The capacitance distribution and placement of ESD devices impacts the CDM current path. The turn-on time of ESD devices and RC delays of connections impacts the discharge time constant.

A. Simplified Charge Distribution Model

In most of our products, the global ground serves as the primary ESD rail for routing CDM currents within the IC. Figure 6 illustrates current flow in the event of CDM stress on an I/O pin. The CDM current is routed to and from the global ground (VSS) grid via ESD diodes and clamps distributed in multiple power domains across the chip. Therefore, the vast majority of the die and package charges on nets other than global VSS, discharge via the global VSS grid. VSS serves as a pathway for the majority of the CDM current as it discharges to the grounded (stressed) pin.

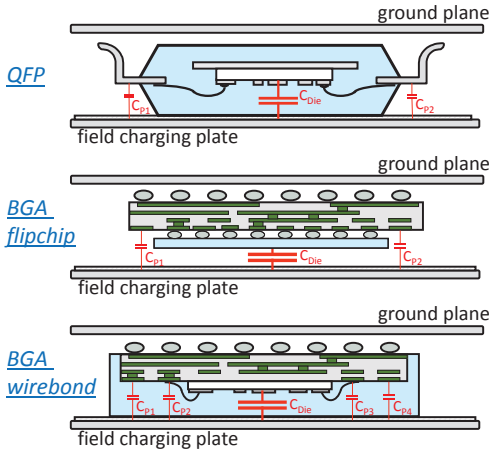

Figure 5: Conceptual drawing of different package types in a FICDM tester setup and the resulting CDM-relevant capacitances.

Considering every detail of the charge distribution in a transient CDM simulation makes a full chip analysis far too complex. But a manageable problem can be achieved with reasonable simplifications.

Hence, for our analysis, we can make the simplifying assumption that the current flow through the global ground net during a CDM event can be simulated with reasonable accuracy by distributing all CDM-relevant current on the global ground net. We will show in Section V that this assumption produces results which correlate well with the observed CDM failures.

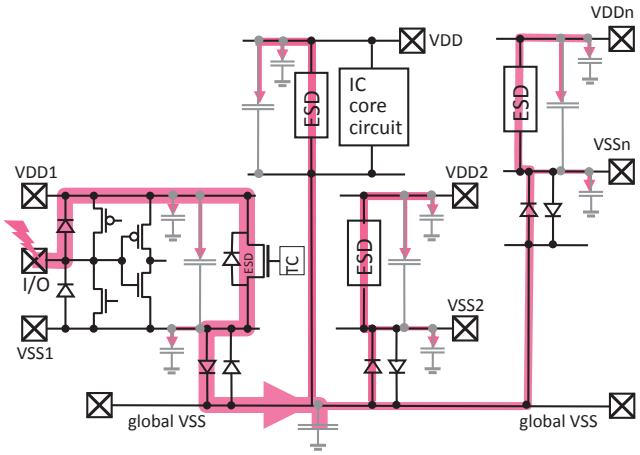

Figure 6: Current distribution through the global ESD node (VSS) during a CDM event on an I/O pad in the VDD1/VSS1 domain.

B. Simplified Current Model

Static vs. transient simulation: A transient simulation would be too computationally intensive. A static simulation method enables the processing of the huge amount of data required for full-chip verification. This simplification does not result in a significant loss of accuracy as resistance is linear. The RC component of the discharge is not covered.

CDM peak current for simulation: A method to extract the total CDM peak current was demonstrated in [5]. For this work, the peak CDM current was determined through interpolation of existing CDM peak current data from similar packages and die sizes.

C. Charge Distribution for Simulation

The CDM current distribution can be implemented in different ways, e.g. distributing current sources:

- Evenly over the complete global ground grid
- Weighted to account for larger areas connected to the ground grid in some areas
- Associated with any distributed layout geometry

This simplification allows for a reasonably accurate CDM-relevant grid analysis with millions of D/R pairs on the chip without package models.

V. CDM Verification Method

A flow chart of the full-chip CDM verification method described in this paper is depicted in Figure 7. It combines a few critical steps for an accurate, CDM-relevant analysis of IC supply grids.

First, current sources are distributed over relevant nets following the method described in Section IV. In addition, a full-chip resistance model of these nets and information about the location of D/R pairs must be extracted. A CDM event is simulated by placing a current sink on one IC pin at a time. The simulation is repeated for all pins, one at a time. For each simulation, D/R pairs with ground voltage drops exceeding the critical voltage limit for oxide failure in the CDM time domain are identified and ordered by voltage. Once simulations for all pins are complete, only the worst case violation for each D/R is reported including information about the discharge pin causing it. Any violations are addressed through design modifications and the updated design is re-verified.

A. Application to Product

In order to prove that the analysis method described in this paper catches potential CDM issues on the chip, it was implemented by using scripts developed on top of a widely-available, commercial IR drop tool. The simulation was performed for the failing product version described in section II on a pin in the North-East (NE) corner, known to cause damage during CDM test. For the analysis, we focused on a correlation between the highest reported voltage drops and the oxide damage locations identified by FA, not on the exact voltage limit. We expected that areas with CDM risk stand out with significantly higher voltages compared to the majority of the chip. Initial simulations were run at 5A and voltage limits were set to a low voltage level (3V). Figure 8 and Table 1

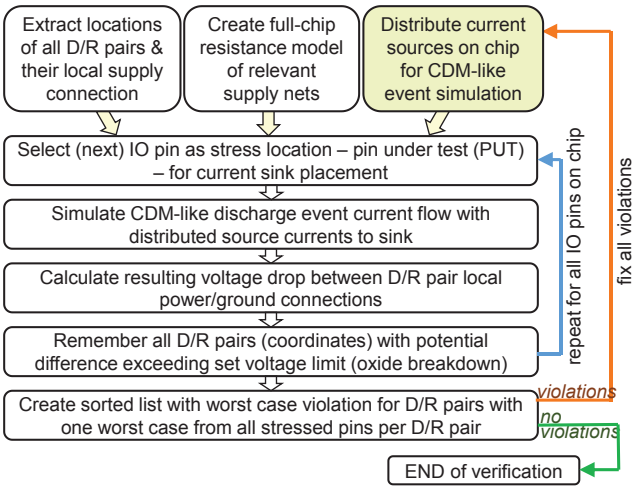

Figure 7: Full chip CDM verification method flow chart.

show the scaled results of this simulation to account for the expected CDM peak current of about 12A for this product. This is applicable as the voltage drop across resistors scale linearly with the current.

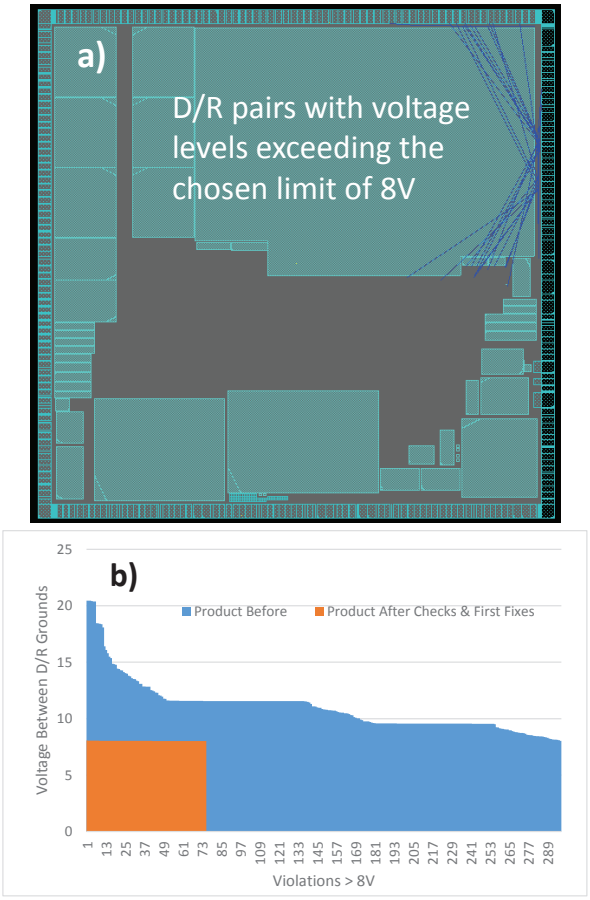

Figure 8: a) Product floorplan. Lines indicate positions of flagged D/R pairs; b) Number of D/R VSS voltage exceeding 8V, sorted highest to lowest. Blue: original design, orange: modified version.

Figure 8 a) shows flylines between the D/R pairs with the highest reported ground voltage. There is good agreement with these locations compared to the oxide damage locations found by FA (compare Figure 1). Figure 8 b) depicts the number of D/R pairs that were flagged as exceeding 8V, sorted highest to lowest. Each reported violation number is plotted on the x-axis and has its associated voltage level plotted on the y-axis. Blue shows the violations in the original design (roughly 300). Orange depicts the violations in the design version after some VSS grid improvements were implemented. There are only about 75 violations left, all close to the set threshold of 8V. D/R pairs with voltages below 8V are not included in the graph. Both the number of violations and the maximum voltage were reduced significantly in the modified design. Table 1 lists the signals with oxide damage identified by failure analysis. All 8 of these signals were reported in the top 50 highest D/R pair voltages

on the chip. An exact correlation (i.e. highest voltage on these locations only) was not expected. One reason is that we are applying simplifications to enable this complex full-chip analysis and the other is that oxide failure has a statistical component. This means that the same transistor may fail on one chip but may not be damaged on the next.

Receiver nets identified by FA	Reported voltage	Reported in top 50 violations
signal_1	22	yes
signal_2	17.5	yes
signal_3	19.3	yes
signal_4	15.4	yes
signal_5	15.4	yes
signal_6	16.2	yes
signal_7	14.9	yes
signal_8	14.6	yes

Table 1: List of signals with damaged gate oxide identified by failure analysis. All were reported in the top 50 reported violations for exceeding the defined oxide breakdown voltage limit.

B. Improving CDM Robustness

In the early product version that failed the initial CDM test, significant improvements to the CDM robustness were achieved by adding more connections between the VSS grid of the main chip and the already existing, but star-routed grid in one of the analog IP. This one change resolved hundreds of violations (Figure 8 b) between the original and the modified design. Adding buffers between D/R pairs exceeding the set voltage threshold to divide the voltage is another option.

Note that placing small local ESD protection for the gate may not be sufficient to protect the oxide from damage if the currents and resistances in that area are too large. Appropriate ESD protection has to be selected. Reducing the grid resistance, if possible, is a much better solution as it typically corrects a large number of related D/R voltage violations.

VI. Commercial EDA Tools

The basic implementation of the verification method described in the previous section proved that the methodology works well to identify failing areas during CDM stress. However, it lacks features required for use in predictive full-chip pre-tapeout verification with hundreds of pins on the chip. For that, more automated and comprehensive EDA tools are needed. To this end, new EDA tools were developed in collaboration with two different tool vendors. The next section describes these tools.

A. ESRA-CDM (SFT)

1. CDM Analysis Details

A methodology for CDM verification of supply nets similar to that described in the previous section was implemented in a commercial software tool ESRA (ElectroStatic discharge Reliability Analyzer) [6]. The ESRA-CDM methodology includes the following steps (also see flow chart in Figure 9).

(1) User defined current level, according to expected CDM peak current, oxide breakdown level in CDM time domain (maximum voltage level allowed), and pin under test (PUT) coordinates.

(2) Resistance extraction for power/ground nets involved in CDM discharge event

(3) DC simulation of the current flow in ground net with the following boundary conditions:

- Distributed current injection to areas on ground net according to their capacitive coupling to the charging plate (see Figure 5), with a user-defined total injection current
- Grounding one pin at a time (CDM PUT)

(4) Voltage differences between local ground points for all D/R pairs on the chip are analyzed. Pairs with voltage differences exceeding the critical value, and the receiver gate net name are flagged, saved in the report file, and can be visualized as flylines on top of the layout (see Figure 10)

(5) To identify the high resistance, weak, or bottleneck areas for current flow in the VSS net for a given grounded pin, potential and current density distributions can be interactively explored using a GUI visualization tool (Figure 12 and 13).

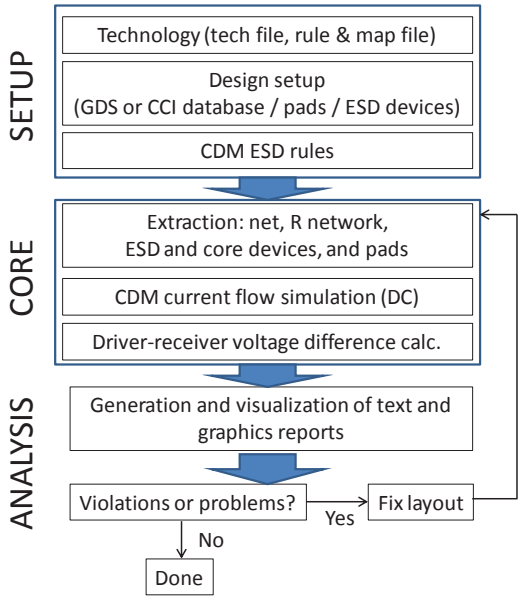

Figure 9: Diagram of the ESRA-CDM simulation flow.

(6) Steps 3-5 are repeated for all user-specified pins on the chip; a summary table with the highest D/R ground point voltage differences is created, for a top-view analysis of the CDM verification results.

Required ESRA-CDM inputs include the Calibre Connectivity Information (CCI) database, technology file (ITF or any other industry standard format for BEOL description), map file, and an input deck with user defined pad locations and CDM peak current.

2. Product Results

The ESRA-CDM methodology has been applied to the original and improved versions of the product described earlier in this paper. The simulation was run with a CDM peak current of 15A and a very conservative voltage limit for the oxides of 5V. Flylines indicating D/R pair locations with the highest VSS voltage differences for the original design are shown in Figure 10. All 8 oxide failures identified by failure analysis after CDM stress were among the reported top 50 D/R pair voltage violations.

Top-level tables (step 6), shown in Figure 11, demonstrate a drastic reduction of the maximum voltage differences on D/R pairs between the failing version (a) and the improved version (b). The second column lists the maximum voltage drop between the pin under test and any other VSS location on the chip. The last column is the maximum voltage drop across a receiver gate during the discharge of that pin in % of the maximum allowed voltage level (set in step 1). The results are sorted by the maximum stress % level. The improved design shows a maximum voltage drop of 9.17V at 15A of CDM current (83.4% above the conservative set maximum voltage level of 5V) across a receiver gate compared to the almost 19V of the original design with oxide failures after CDM stress.

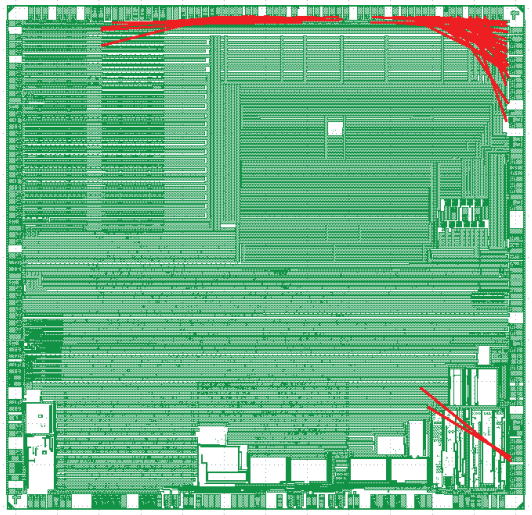

Figure 10. Flylines showing D/R pairs with highest voltage differences for the original design.

ID	NAME	V	STRESS,%
199	CDM_gnd_pin_61	21.98	279
203	CDM_gnd_pin_57	21.67	268
86	CDM_gnd_pin_174	22.01	267
195	CDM_gnd_pin_65	21.88	267
161	CDM_gnd_pin_99	22.01	264
88	CDM_gnd_pin_172	21.37	258
173	CDM_gnd_pin_87	21.7	256
238	CDM_gnd_pin_22	22.12	255
87	CDM_gnd_pin_173	21.52	253
160	CDM_gnd_pin_100	21.17	245
104	CDM_gnd_pin_156	20.74	236

a)

ID	NAME	V	STRESS,%
151	CDM_gnd_pin_109	12.08	83.4
152	CDM_gnd_pin_108	11.98	79
108	CDM_gnd_pin_152	12.25	76.3
149	CDM_gnd_pin_111	12.47	75.2
106	CDM_gnd_pin_154	12.39	74.9
147	CDM_gnd_pin_113	12.5	74.2
216	CDM_gnd_pin_44	11.85	74
153	CDM_gnd_pin_107	11.71	73.3
145	CDM_gnd_pin_115	12.33	71.8
146	CDM_gnd_pin_114	12.34	71.2

b)

Figure 11: Summary tables for the top D/R pair voltage difference violations for (a) original and (b) improved product designs.

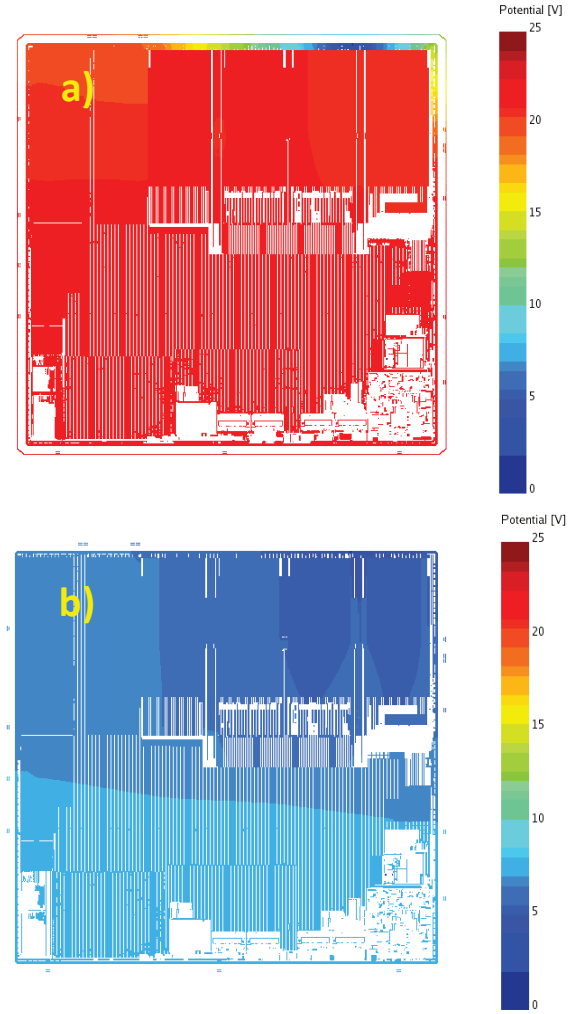

Figure 12. Potential distributions for (a) original and (b) improved layout for grounded pin 61 (see Figure 11 a).

Selecting any row in the table shown in Figure 11 will open a detailed list of the D/R pairs with voltage differences exceeding the user set maximum value and their coordinates. This information is sufficient to locate problematic areas in the ground grid and define solutions to solve the issues. However, this tool also provides a visualization of the current flow and potential map to further assist with the debugging of potential issues. Figure 12 shows the potential distributions in the metal 4 layer for a simulated discharge of one pin in the NE corner of the chip. Figure 13 depicts current densities in all metal layers for the same pin under test. The improved design has a significantly reduced maximum VSS net voltage as the implemented layout improvements result in a reduced net resistance. Peak current densities are also reduced and the current is distributed more evenly.

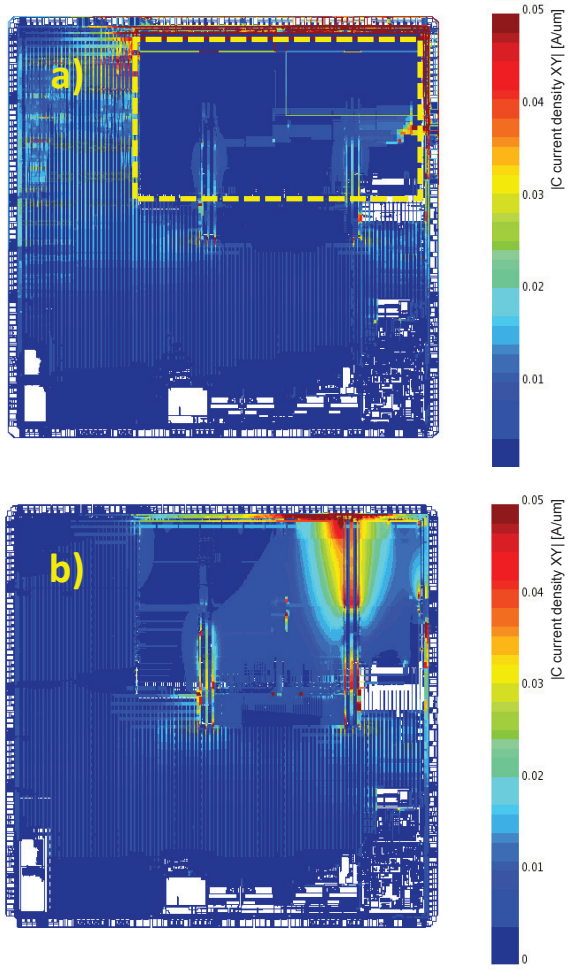

Figure 13. Current density distributions in all metal layers for (a) original and (b) improved layouts.

Note that the voltage and current density map feature can be used in earlier design stages, e.g. during the power/ground grid floorplanning stage, before netlists and layout with exact D/R pair locations are available.

B. Pathfinder-S (Ansys)

1. CDM Analysis Flow

A check for verifying the ground grid for CDM robustness as described in Section V was also implemented in the commercial software tool Pathfinder-S(static). The latter is a layout based ESD integrity analysis solution that performs checks typically focused on ESD robustness in primary ESD discharge paths. Figure 14 describes the flow for performing driver-receiver checks for ensuring CDM robustness of the global ground network.

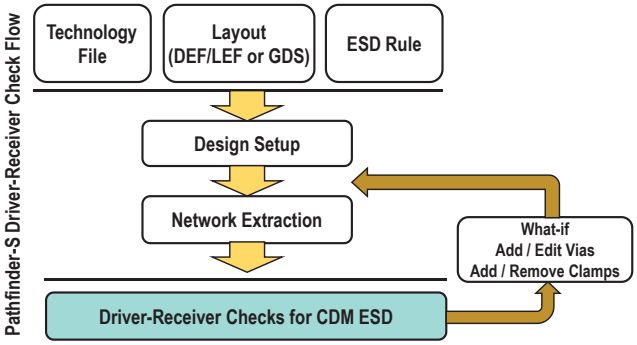

Figure 14: Driver-Receiver check flow using Pathfinder-S.

The tool reads the standard place-and-route database in LEF/DEF format, the technology file for parasitic extraction of the power/ground network, an ESD rule file including user defined variables, and a list of the pin names and coordinates for all IO pads. For a full-chip CDM analysis, two check types are available.

- Driver-receiver ground resistance checks
- Driver-receiver ground differential voltage checks

2. Driver-Receiver Resistance Check

The user defines the maximum resistance (R_{max}) allowed between D/R ground pins. The check identifies all D/R pairs from the design, performs the ground network extraction, and computes the effective resistance between the local ground nodes. D/R pairs which exceed R_{max} are listed in a text report and can be located in the GUI as shown in Figure 15 a.

This check revealed several potential weaknesses in the product described in this paper. For example, a few paths were highlighted that are on the south side of the chip. Issues can be further analyzed using the Shortest-Path Tracing (SPT) feature which provides a detailed breakup of wires and vias by segment of the least resistance path for the flagged D/R pairs. It reveals that in the case shown in Figure 15 b, the high D/R resistance is caused by missing Via1.

Note that no gate oxide failures were found in this area after CDM stress. As described in Section 3.B,

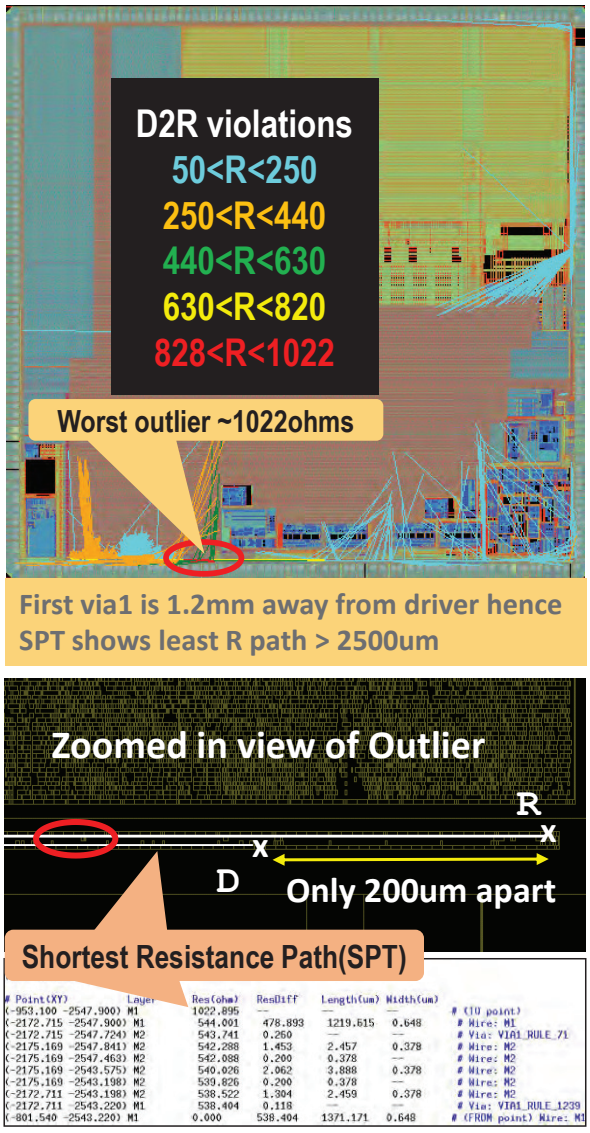

Figure 15 a (top): Product driver-receiver resistance check results; b (bottom) tools for debugging violations. D: Driver, R: Receiver.

detecting potential CDM failure paths based just on a resistance constraint will flag many paths that are not actually vulnerable for CDM if there is no high CDM current flow through the same area.

This again emphasizes the need for taking a realistic current distribution into account for a CDM relevant ground grid analysis. The D/R resistance checks can still provide very useful information to improve the robustness of the ground grid and can be used to remove any gross errors in the layout that might cause potential ESD issues. For example, the areas that had gate oxide damage after CDM stress are flagged as having a very high resistances between the D/R pairs. The main advantage of the resistance check is that it can be performed at the synthesizable sub-block level, while the differential voltage checks are dependent on the IO pad hook-up to the global ground network.

3. Driver-Receiver Voltage Check

The driver-receiver voltage check provides more CDM relevant results by taking the current flow in the global ground domain during CDM discharge into account as shown in Figure 16.

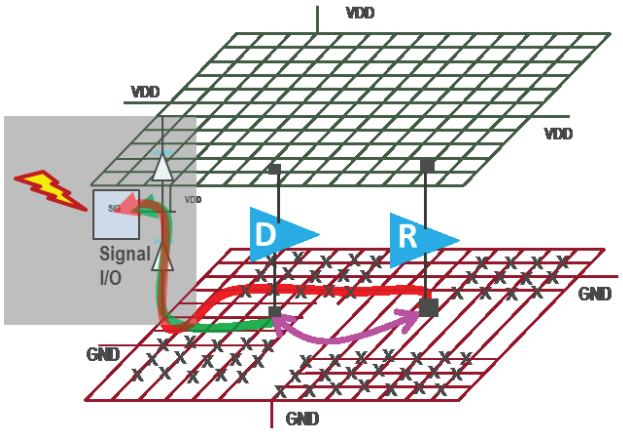

Figure 16: D/R differential voltage check implementation. D: driver, R: receiver, x: current source distribution. Red: current path from receiver, Green: current path from driver, Purple: voltage between the local ground pins of driver and receiver.

In order to perform this check the following inputs must be provided:

(1) Peak CDM current and layer in which current sources should be distributed

(2) Failure threshold in Volts for D/R pair

(3) List of IOs (pin names) along with global ground coordinates

Pathfinder-S extracts the ground network, identifies all D/R pairs and retains them as probing points. The network is formulated with the user defined CDM peak current distributed as current sources on the user specified layer and a current sink at the global ground pin of every IO pad. During the analysis, each pin under test (each IO) is zapped one at a time as shown in Figure 16. The ground pin voltage is monitored on every driver-receiver pair and compared against the user defined voltage threshold (oxide breakdown in CDM time domain). Any driver-receiver violation during each zap is retained. Once the tool simulated all IO pads, it provides a consolidated list of D/R pairs that failed the differential voltage check during simulation. Signal names and coordinates, which are needed to improve the existing design, are included.

The differential voltage checks provided CDM relevant result for the product discussed in this paper. Figure 17 summarizes the driver-receiver differential voltage results. The histogram (Figure 17 bottom) shows driver-receiver pairs that are exceeding the failure constraints. The biggest outliers were between

10-14V differential voltages (at 5A CDM current) and as shown in the GUI, all those outliers are around the periphery of the large IP block at the top right, which indicates some ground weaknesses nearby. These weaknesses correlated well with silicon measurements and hence proves that driver-receiver differential voltage checks can help in identifying the outliers in more accurate way. The SPT feature described in Figure 15 can be used to identify layout bottlenecks in the D/R pair differential voltage checks.

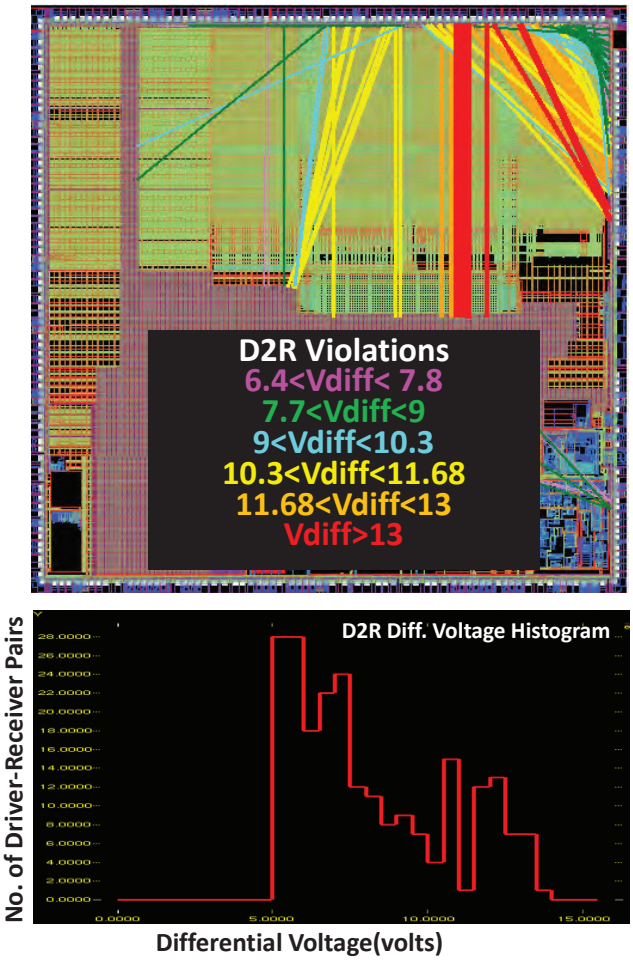

Figure 17: D/R pair differential voltage check results.

As a recommended ESD design methodology, the driver-receiver resistance checks can be adopted early on in the design flow, possibly with relaxed constraints. Any severe violations, for example due to issues in the floor planning or discontinuities in the ground grid, can be fixed at this stage. Once the full chip is assembled, including the IO ring, the differential voltage checks can be performed to detect any D/R pairs that are vulnerable to CDM discharge. Results flagged by the D/R voltage check have a high relevance for CDM failures but are likely not revealed by typical EMIR analysis or current density checks.

C. EDA Tool Result Conclusions

Note that the results for the same database vary slightly between the different EDA tools. This is due in part to the simplified current distribution model utilized. In addition, the two commercial EDA tools differ in how they process data, and different parts of the chip were included in the analysis due to the nature of the EDA tool used. But the key point is that, for both tools, all 8 gate oxide failures identified by failure analysis were in the top 50 reported violations.

The simulations with the commercial EDA tools are highly automated and require only basic input information from the user. Areas that are at high risk for gate oxide failures during CDM discharges are reliably identified. Once the details of potential issues are known, they can typically be resolved easily with minor power/ground grid modifications.

The most impressive result however is that these tools are able to process a huge amount of data – the analyzed product includes 7 metal layers, an area of 30 mm^2, 4.14 million D/R pairs, and approximately 260 I/O pads – in a very reasonable amount of time, i.e. in less than 24h. For both tools, results can be produced even faster by running parallel processes, e.g. to analyze larger SOCs in a reasonable time frame. The tools produce results that are essential to avoid CDM oxide damage, especially for mixed signal chips with sensitive isolated analog grounds.

D. Product results

We used the commercial EDA tools to improve the VSS grid of the early product version before tape-out of the product. We applied a CDM peak current of 12A with a D/R pair maximum voltage drop of 5V. We expect that the product will easily pass 500V CDM (AEC). We have successfully used these EDA tools for several products since then and were able to resolve several issue with high risk for CDM damage.

E. Limitations and Further Work

In the product example described in this paper, limiting the analysis to one global ground net was sufficient. In fact, due to the ESD protection strategy used for most of our designs, this approach is sufficient for the majority of our products. However, for integrated circuits that have several separate ground nets as ESD nodes connected through anti-parallel ESD diodes as shown in Figure 18, the method can be extended to cover multiple grounds on the chip. In some cases, it may benefit the accuracy of the results to include power grids as well. For this extended application, active ESD devices must be

included in the simulation as shown in Figure 19. In addition, the analysis currently relies on identifying the closest ground pin to any pin under test to run the analysis. Including ESD devices in the analysis simplifies setup requirements as only IO pad coordinates need to be specified. Since ESD devices typically have different resistances depending on the polarity of the current flow, this will have to be considered if ESD devices are included.. The tools discussed in this paper already have the framework for supporting ESD devices and therefore an extension to multiple supply domains should be fairly easy to implement and is currently in development.

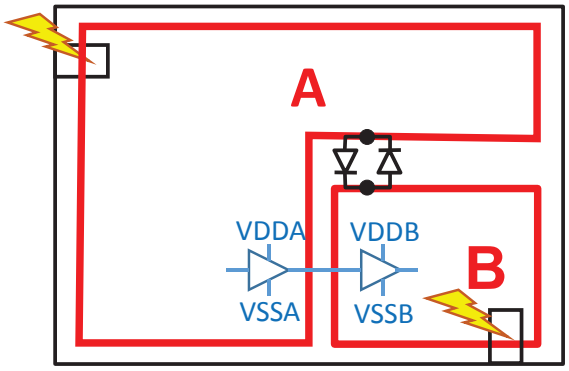

Figure 18: Product with separate ground grids as local ESD nets connected through anti-parallel ESD diodes. For proper full-chip CDM analysis, both grounds and ESD diodes must be considered.

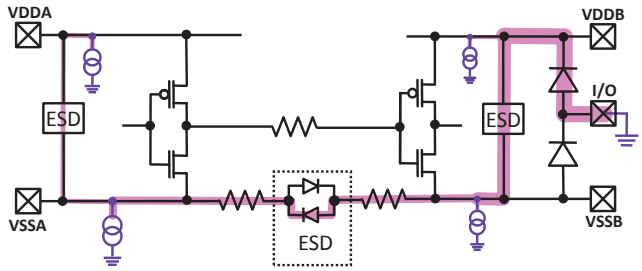

Figure 19: Simplified CDM current flow through multiple supply nets connected through ESD devices.

F. D/R Supply Domain Crossings

Once the commercially available tools are extended to cover multiple ground and potentially also power nets, the method can also help to determine appropriate protection for supply domain signal crossings. Netlist based checks can only provide information about the existence of a supply domain signal crossing, but this new verification methodology can provide powerful new insight into the extent of the voltage drop at this crossing during an actual CDM event. This enables selection of appropriate ESD protection devices at affected domain signal crossings. Note that we have found failures on ground-domain signal crossings with proper ESD protection due to excessive voltages during CDM caused by large ground resistances.

VII. Conclusions

This paper introduced a new full-chip CDM ESD verification method that enables the evaluation of millions of driver-receiver pairs for CDM risk. The implementation was made possible by a combination of the computational power of latest EDA tools and simplifications in the CDM simulation approach that led to very good correlation with actual failure modes. When this method was applied to a product with oxide damage in the core region within one power/ground domain, the failing gate oxide locations were correctly identified. It has been used to evaluate several products before tape-out and in some cases high risk areas were found and easily corrected with local ground grid improvements. Planned enhancements of the commercial EDA tools to add active ESD devices in the analysis will enable the expansion of the tool to different ground and power nets and will make this method applicable for all designs. We have found this an extremely valuable tool to ensure first-time-right ESD designs for any complex IC.

References

[1] Mototsugu Okushima, Tomohiro Kitayama, Susumu Kobayashi, Tetsuya Kato and Morihisa Hirata, “Cross Domain Protection Analysis and Verification using Whole Chip ESD Simulation”, 2010 IEW.

[2] Harald Gossner, Gautam Singampalli, Harshit Dhakad, “Can ERC-based Formal Verification Supersede CDM Simulation?”, 2013 IEW.

[3] Dolphin Abessolo-Bidzo, Theo Smedes, Albert Jan Huitsing, “CDM Simulation Based on Tester, Package and Full Integrated Circuit Modeling: Case Study”, IEEE TED, v. 59, n. 11, 2012.

[4] Vrashank Shukla, Nathan Jack, Elyse Rosenbaum, “Predictive Simulation of CDM Events to Study Effects of Package, Substrate Resistivity and Placement of ESD Protection Circuits on Reliability of Integrated Circuits”, IRPS 2010.

[5] Vrashank Shukla, Gianluca Boselli, Mariano Dissegna, Charvaka Duvvury, Raj Sankaralingam, Elyse Rosenbaum, “Prediction of Charged Device Model Peak Discharge Current for Microelectronic Components”, IEEE TDMR, v. 14, n. 3, 2014.

[6] Maxim Ershov, Yuri Feinberg, Meruzhan Cadjan, David Klein, and Melanie Etherton, “EDA software for verification of metal interconnects in ESD protection networks at chip, block, and cell level”, ESD Symp. Proc., 2013.